CLAIMS

What is claimed is:

1. A memory array comprising:

a plurality of two-terminal memory plugs, each two-terminal memory plug operable to change from a high resistive state to a low resistive state upon application of a first write voltage and change from a low resistive state to a high resistive state upon application of a second write voltage, and each two terminal memory plug including a multi-resistive state element that includes a conductive element and a reactive metal that reacts with the conductive element.

2. The memory array of claim 1, wherein the reactive metal has fully reacted with the conductive element.

3. The memory array of claim 1, wherein each two-terminal memory plug includes a bottom electrode at one of the terminals and a top electrode at the other terminal.

4. The memory array of claim 3, wherein:

the bottom electrode is deposited before the conductive element;

the reactive metal is deposited on the conductive element after deposition of the conductive element; and

the top electrode is deposited after the deposition of the reactive metal.

5. The memory array of claim 4, wherein no portion of the reactive metal between the conductive element and the top electrode is unreacted with the conductive element.

6. The memory array of claim 4, wherein an anneal step is used after deposition of the reactive metal and prior to deposition of the top electrode.

7. The memory array of claim 4, wherein an anneal step is used after deposition of both the reactive metal and the top memory electrode.

8. The memory array of claim 1, wherein each two-terminal memory plug can be exposed to a range of voltages without disturbing the resistive state of the memory plug.

9. The memory array of claim 1, wherein the multi-resistive state element is substantially non-conductive over a range of voltages from V_{NO-} to V_{NO+}.

10. The memory array of claim 9, wherein a manganite perovskite is used as the conductive element.

11. The memory array of claim 10, wherein the manganite perovskite is a PCMO.

12. The memory array of claim 11, wherein a reactive metal that can react with the PCMO is Al, Ti, Mg, W, Fe, Cr, Vn, Zn, Ta or Mo.

13. The memory array of claim 12, wherein the reactive metal is Al.

14. The memory array of claim 12, wherein 10 - 100 Angstroms of Al is deposited on the PCMO.

15. The memory array of claim 14, wherein 25 - 50 Angstroms of Al is deposited on the PCMO.

16. A process for fabricating memory plugs comprising:

depositing a bottom electrode;

depositing a conductive metal oxide;

depositing a very thin layer of material on the conductive metal oxide ; and

depositing a top electrode;

wherein the memory plug is reversibly programmable to different resistive states.

17. The process of claim 16, wherein the very thin layer of material is Al, Ti, Mg, W, Fe, Cr, Vn, Zn, Ta or Mo.

18. The process of claim 16, wherein the top electrode is Pt.

19. A re-writable memory comprising:

a memory array including a plurality of memory cells, each memory cell having a memory plug that includes a multi-resistive state element, the multi-resistive state element having a conductive element and a very thin layer of material that is less

than 200 Angstroms thick, the memory plug being capable of reversibly switching from a first resistance state to a second resistance state; and

peripheral circuitry capable of selecting certain memory cells out of the memory array to either determine the resistive states of the memory plugs within the selected memory cells or cause the memory plugs within the selected memory cells to switch states.

20. The memory array of claim 19, wherein the material is fully reacted with the conductive element.

21. The memory array of claim 19, wherein each memory plug can be exposed to a range of voltages without disturbing the resistive state of the memory plug.

22. The memory array of claim 19, wherein each memory plug includes at least two electrodes.

23. The memory array of claim 22, wherein the conductive element is a conductive metal oxide.

24. The memory array of claim 23, wherein the very thin layer of material is Al, Ti, Mg, W, Fe, Cr, Vn, Zn, Ta or Mo.

25. The memory array of claim of claim 24, wherein at least one of the electrodes is Pt.

26. The memory array of claim 19, wherein the multi-resistive state element has a non-ohmic characteristic such that the multi-resistive state element exhibits:

a high resistance regime for a range of voltages; and

a resistance associated with the resistive state for voltages outside of the range of voltages.